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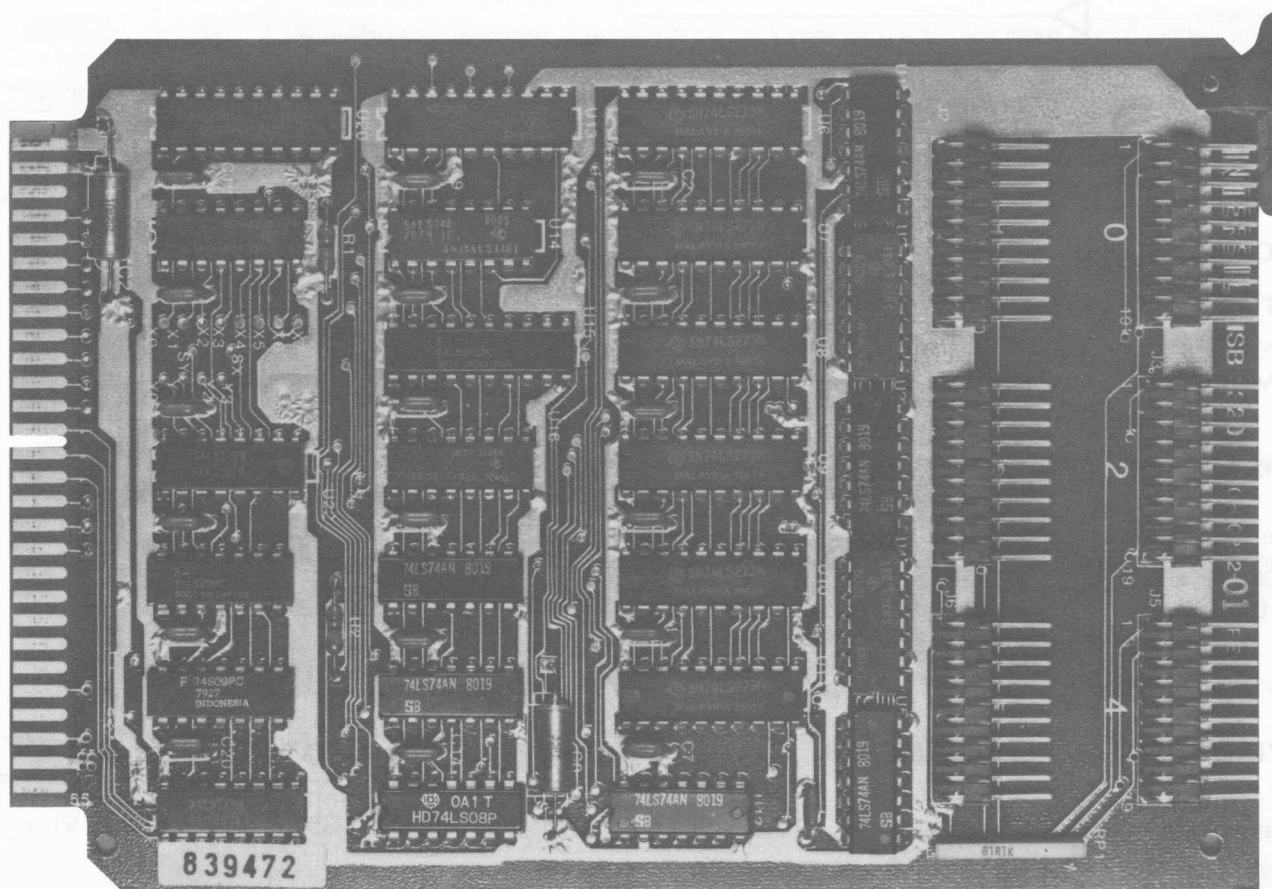
### FEATURES

- Full STD Bus Compatibility
- Six 8-Bit Output Ports
- Interrupt Capability with Polling Identification
- Two Handshake Lines per Port
- Customer Selectable Addresses of Six Consecutive Output Ports
- Input Loading of One Low-power Schottky Load
- Data Output Drive of 60 Low-power Schottky Loads
- Priority Encoded Port Status Register
- Single +5V Operation

### GENERAL DESCRIPTION

The ISB-3320 is a STD BUS Interface Card that provides 6 fully buffered and latched parallel output ports. Each port is one byte (8 bits) wide. The card will operate with virtually any STD BUS Microprocessor Card (Z80, 6800, 8080, 8085, 8748, etc.). It is totally compatible with the ISB-3100 and the ISB-3110 Central Processor Cards.

Each of the six output ports has two TTL compatible handshake lines that enable the user to control the data handled through that port. An interrupt is generated at the discretion of the customer by sending the handshake signal, Control Handshake Signal In (CHSIN) having a transition from a logic 0 to logic 1, to the port. The Interrupt status register will indicate which one of the ports interrupted the CPU. The ports are prioritized with port 0 having the highest priority and port 5 having the lowest priority. Ports 6 and 7, although addressable, are not used. All data output lines are latched and can drive 60 low power Schottky loads. The customers interface to a port is through a 20-pin header. One header for each port.



# ISB-3320

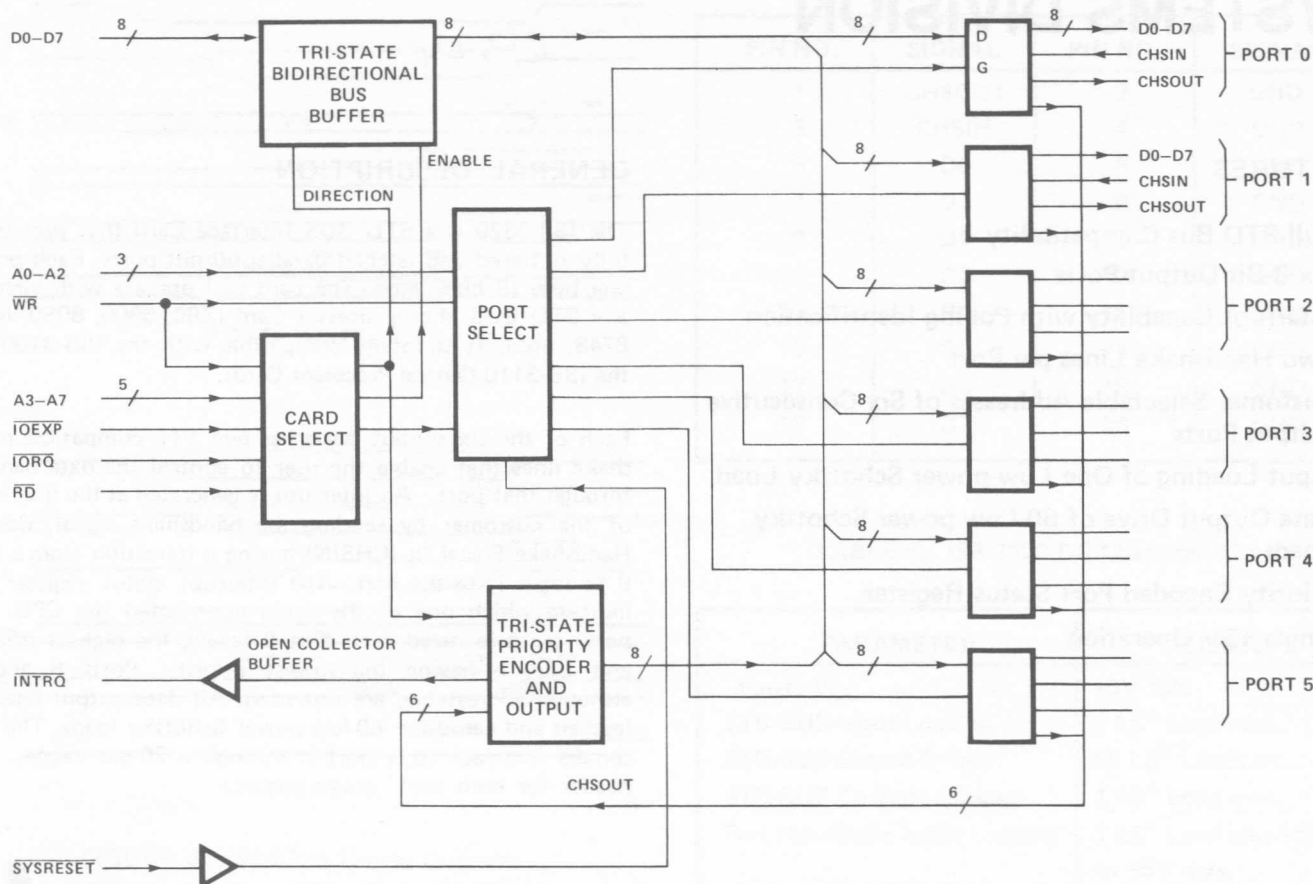


FIGURE 1. ISB-3320 Block Diagram

## SPECIFICATIONS

Word Size:	8 Bits
Capacity:	6 TTL Compatible Ports
I/O Address Selection:	Lowest Port Address Selectable within the range of 00 and F8, in increments of 8.
Interface:	All Address, Data and Command Signals are TTL Compatible.
Power Requirements:	5 VDC at 0.5 Amp max.
Mating Connectors:	See Table 1
Card Dimensions:	Height 6.5 inches (16.51 cm) Width 4.48 inches (11.38 cm) Thickness: 0.442 inches (1.122 cm)

## ENVIRONMENTAL REQUIREMENTS

Operating Temperature:	0° to 55°C
Storage Temperature:	-40° to 80°C
Relative Humidity:	0% to 90% without condensation.

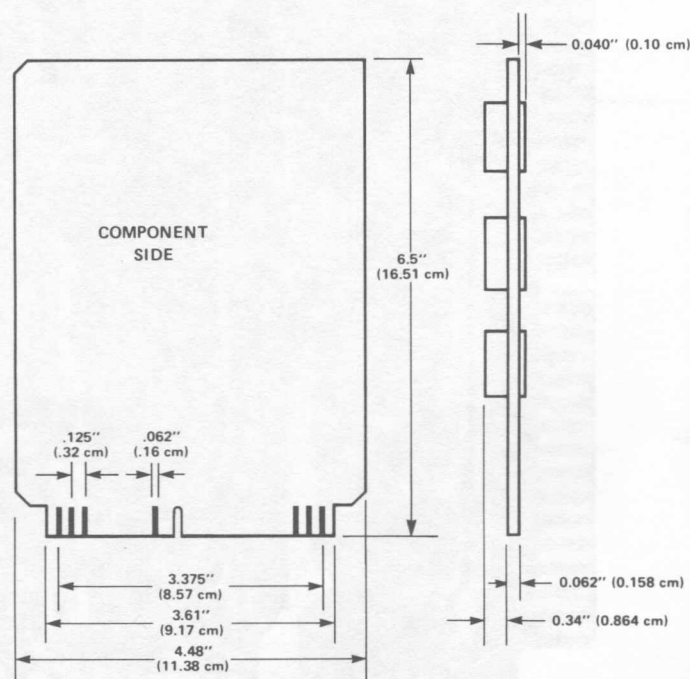


FIGURE 2. ISB-3320 Card Dimensions

TABLE 1. ISB-3320 Compatible Mating Connectors

INTERFACE	NO. OF PINS	CENTERS	CONNECTOR TYPE	VENDOR	VENDOR PART NO.	KEYED
STD BUS	56	0.125 in.	Solder Tail	Viking Winchester	VH28/ICNK5 2HW D0-111	Between Pins 26 and 28
STD BUS	56	0.125 in.	Wire Wrap	Viking Winchester	VH28/ICND5 HW28 D0-111	Between Pins 26 and 28
I/O Header Connector	20	0.100 in.	Solder Tail	AMP Robinson Nugent T & B/ Ansley	88376-2 1 DS-20 609-2000	N/A

TABLE 2. ISB-3320 STD BUS Organization and Functional Specifications (With Pin Definitions)

The STD BUS pinout is organized into five functional groups:

Logic Power Bus	Pins 1-6
Data Bus	Pins 7-14
Address Bus	Pins 15-30
Control Bus	Pins 31-52
Auxiliary Power Bus	Pins 53-56

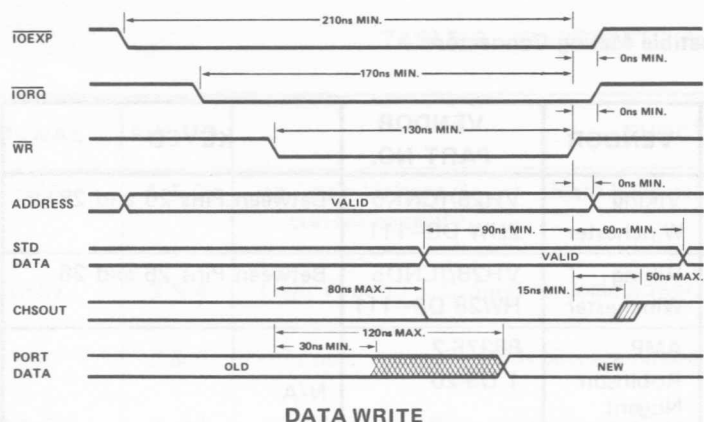
COMPONENT SIDE				CIRCUIT SIDE			
PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
1	+5V	In	+5 Volts DC (Bussed)	2	+5V	In	+5 Volts DC (Bussed)
3	GND	In	Digital Ground (Bussed)	4	GND	In	Digital Ground (Bussed)
5	-5V	In	-5 Volts DC	6	-5V	In	-5 Volts DC
7	D3	In/Out	Low Order Data Bus	8	D7	In/Out	High Order Data Bus
9	D2	In/Out	Low Order Data Bus	10	D6	In/Out	High Order Data Bus
11	D1	In/Out	Low Order Data Bus	12	D5	In/Out	High Order Data Bus
13	D0	In/Out	Low Order Data Bus	14	D4	In/Out	High Order Data Bus
15	A7	Out	Low Order Address Bus	16	A15	Out	High Order Address Bus
17	A6	Out	Low Order Address Bus	18	A14	Out	High Order Address Bus
19	A5	Out	Low Order Address Bus	20	A13	Out	High Order Address Bus
21	A4	Out	Low Order Address Bus	22	A12	Out	High Order Address Bus
23	A3	Out	Low Order Address Bus	24	A11	Out	High Order Address Bus
25	A2	Out	Low Order Address Bus	26	A10	Out	High Order Address Bus
27	A1	Out	Low Order Address Bus	28	A9	Out	High Order Address Bus
29	A0	Out	Low Order Address Bus	30	A8	Out	High Order Address Bus
31	$\overline{WR}$	Out	Write to Memory or I/O	32	$\overline{RD}$	Out	Read to Memory or I/O
33	$\overline{IORQ}$	Out	I/O Address Select	34	$\overline{MEMRQ}$	Out	Memory Address Select
35	$\overline{IOEXP}$	In/Out	I/O Expansion	36	$\overline{MEMEX}$	In/Out	Memory Expansion
37	$\overline{REFRESH}$	Out	Refresh Timing	38	$\overline{MCSYNC}$	Out	CPU Machine Cycle Sync
39	$\overline{STATUS 1}$	Out	CPU Status	40	$\overline{STATUS 0}$	Out	CPU Status
41	$\overline{BUSAK}$	Out	Bus Acknowledge	42	$\overline{BUSRQ}$	In	Bus Request
43	$\overline{INTAK}$	Out	Interrupt Acknowledge	44	$\overline{INTRQ}$	In	Interrupt Request
45	$\overline{WAITRQ}$	In	Wait Request	46	$\overline{NMIRQ}$	In	Non-Maskable Interrupt
47	$\overline{SYSRESET}$	Out	System Reset	48	$\overline{PBRESET}$	In	Push Button Reset
49	$\overline{CLOCK}$	Out	Clock from Processor	50	$\overline{CNTRL}$	In	AUX Timing
51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
53	AUX GND	In	AUX Ground (Bussed)	54	AUX GND	In	AUX Ground (Bussed)
55	AUX+V	In	AUX Positive (+12 Volts DC)	56	AUX-V	In	AUX Negative (-12 Volts DC)

TABLE 3. ISB-3320 STD BUS Signal Definitions

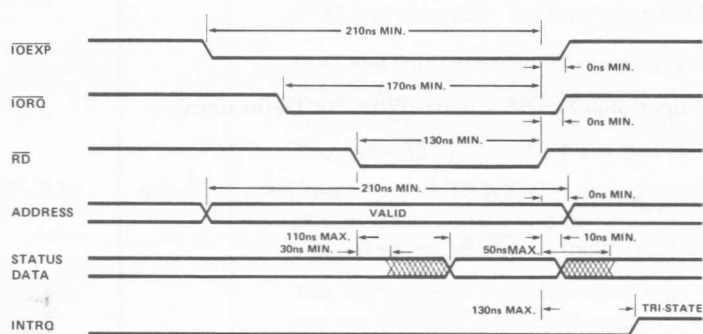
SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
+5V	1 & 2	<i>+5 Logic Voltage (<math>V_{CC}</math>)</i> — Main logic voltage lines (+5 volts). Both pins are bussed together for current capacity.
GND	3 & 4	<i>Logic Ground</i> — Ground for logic power. Both pins are bussed together for current capacity.
-5V	5 & 6	<i>-5 Logic Voltage</i> — Both pins are bussed together for current capacity.
D0-D7	7-14	<i>Data Bus</i> — An 8-Bit bidirectional tri-state bus. (Bidirectional means signals may flow either into or out of any card on the Bus). Direction of data is normally controlled by the processor card via the Control Bus. The data direction is normally affected by such signals as Read ( $\overline{RD}$ ), Write ( $\overline{WR}$ ) and Interrupt Acknowledge ( $\overline{INTAK}$ ).  The Data Bus uses high-level active logic levels. All cards are required to release the bus to a high impedance state when not in use. The Processor card releases the data bus in response to Bus Request ( $\overline{BUSRQ}$ ) input from an alternate system controller, as in DMA transfers. The ISB-3320 uses the Data Bus during I/O Write or I/O Read cycles.
A0-A15	15-30	<i>Address Bus</i> — A 16-bit tri-state high-level active bus. The address will originate at the processor card or a bus controlling device. The processor card releases the Address Bus in response to a Bus Request ( $\overline{BUSRQ}$ ) input from an alternate controller.  The Address Bus provides 16 address lines for decoding by either memory or I/O. Memory request ( $\overline{MEMRQ}$ ) and I/O request ( $\overline{IORQ}$ ) control lines are used to distinguish between the two operations. The ISB-3320 uses the lower 8 bits of the Address Bus during an I/O Request operation.
$\overline{WR}$	31	<i>Write to Memory or I/O</i> — A tri-state, active-low control line that indicates the BUS holds valid data to be written in the addressed memory or output device. The ISB-3320 is an I/O device only.
$\overline{RD}$	32	<i>Read from Memory or I/O</i> — A tri-state, active-low control line that indicates the processor or other bus controlling device wants to read data from memory or an I/O device. The selected I/O device or memory should use this signal to gate data onto the BUS. The ISB-3320 is an I/O device only.
$\overline{IORQ}$	33	<i>I/O Address Select</i> — A tri-state, active-low processor output control line. $\overline{IORQ}$ indicates that the address lines hold a valid I/O address for an I/O Read or Write.
$\overline{MEMRQ}$	34	<i>Memory Address Select</i> — A tri-state, active-low memory request line. $\overline{MEMRQ}$ indicates that the Address Bus holds a valid address for memory read or memory write operations. (Not used on the ISB-3320).
$\overline{IOEXP}$	35	<i>I/O Expansion</i> — An active-low control signal used to expand or enable I/O Port addressing.
$\overline{MEMEX}$	36	<i>Memory Expansion</i> — An active-low control signal used to expand or enable memory addressing. (Not used on the ISB-3320).
$\overline{REFRESH}$	37	<i>Dynamic Memory Refresh</i> — a tri-state, active-low control line normally used to refresh dynamic memory. This signal is generated on the processor card. (Not used on the ISB-3320).
$\overline{MCSYNC}$	38	<i>Machine Cycle Sync</i> — A tri-state, active-low processor output signal that occurs once during each processor machine cycle. (Machine cycle is defined as the sequence that involves Addressing, Data Transfer and Execution.) $\overline{MCSYNC}$ defines the beginning of the machine cycle. (Not used on the ISB-3320).
$\overline{STATUS\ 1}$	39	<i>Status Control Line 1</i> — (Not used on the ISB-3320).

TABLE 3. ISB-3320 STD BUS Signal Definitions (Continued)

SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
STATUS 0	40	<i>Status Control Line 0</i> — Status Control lines provide timing information related to special cycle operations. (Not used on the ISB-3320).
BUSAK	41	<i>BUS Acknowledge</i> — An active-low output line. The processor responds to a $\overline{\text{BUSRQ}}$ by releasing the BUS and giving an Acknowledge signal on the BUSAK line. BUSAK occurs at the completion of the current machine cycle. (Not used on the ISB-3320).
BUSRQ	42	<i>Bus Request</i> — An active-low input line. A $\overline{\text{BUSRQ}}$ causes the processor to suspend operations on the BUS by releasing all tri-state BUS lines for use by another processor. The BUS is released once the current machine cycle is completed. (Not used on the ISB-3320).
INTAK	43	<i>Interrupt Acknowledge</i> — An active-low output line from the processor card that occurs in response to ( $\overline{\text{INTRQ}}$ ). It is used to tell the interrupting device that the processor card is ready to respond to the Interrupt. For vectored interrupts the vector address is placed on the Data Bus by the interrupting device during INTAK. (Not used on the ISB-3320).
INTRQ	44	<i>Interrupt Request</i> — An active-low processor card input line that conditionally interrupts the program. It is masked and ignored by the processor unless deliberately enabled by a program instruction. If the processor accepts the interrupt, it acknowledges by dropping INTAK.
WAITRQ	45	<i>Wait Request</i> — An active-low input line to the processor that suspends processor operations as long as it remains low. The processor will hold in a state that maintains a Valid Address on the Address Bus. (Not used on the ISB-3320).
NMI RQ	46	<i>Non-Maskable Interrupt</i> — An active-low processor card interrupt input line of highest priority. (Not used on the ISB-3320).
SYSRESET	47	<i>System Reset</i> — An active-low output from the system reset circuit. The system reset circuit is triggered by power-on detection or by the pushbutton reset. The system reset bus line should be applied to all cards on the BUS that have latch circuits requiring initialization. The ISB-3320 card has all Output Port Data lines, CHSOUT lines and Interrupts cleared.
PBRESET	48	<i>Push Button Reset</i> — An active-low input line to the system reset circuit. (Not used on the ISB-3320).
CLOCK	49	<i>Clock From Processor</i> — A buffered processor clock signal used for system synchronization or as a general clock source. (Not used on the ISB-3320).
CNTRL	50	<i>Control</i> — An external clock input for special clock timing. (Not used on the ISB-3320).
PCO	51	<i>Priority Chain Output (Output, active-high)</i> — This signal is sent to the PCI input of the next lower card in the priority chain. A card that needs priority should hold PCO low.
PCI	52	<i>Priority Chain In (Input, active-high)</i> — This signal is provided directly from the PCO of the next higher card in the priority chain. A high level on PCI gives priority to the card sensing the PCI input.
AUX GND	53 & 54	<i>Auxiliary Ground</i> — Ground for AUX Power. Both pins bussed together for current capacity.
AUX +V	55	<i>Auxiliary Positive Voltage (+12 Volts DC)</i>
AUX -V	56	<i>Auxiliary Negative Voltage (-12 Volts DC)</i>



DATA WRITE



STATUS READ

**FIGURE 3. ISB-3320 Timing Diagrams**

**TABLE 4. ISB-3320 I/O Connector Pin List**

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	CHSOUT	2	GND
3	CHSIN	4	GND
5	D0	6	GND
7	D1	8	GND
9	D2	10	GND
11	D3	12	GND
13	D4	14	GND
15	D5	16	GND
17	D6	18	GND
19	D7	20	GND

TABLE 5. ISB-3320 DC Characteristics

PARAMETER	LIMITS
Power V <sub>CC</sub>	+5V ±5%
STD BUS Input Loading	1 LS* Load max.
STD BUS Output Drive	60 LS* Loads max.
STD BUS Tri-State Leakage	1 LS* Load max.
Port Handshake Input Loading	1 LS* Load plus 1kΩ to +5V max.
Port Handshake Output Drive	50 LS* Loads max.
Port Data Bus Output Drive	60 LS* Loads max.

\* Low power Schottky

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